MGA-445343-99

4.4 – 5.3 GHz 20W High Efficiency Linear Power Amplifier
Preliminary Data Sheet
Oct 2010

Features:

- **13 dB Gain**
- **43 dBm P_{-3dB}**
- **35 dBm Linear Pout @ 2.5% EVM (802.11 64QAM)**
- **20% Efficiency at 35 dBm Linear Output Power**
- **Fully Matched Input and Output for Easy Cascade**
- **+ 28V Bias Voltage**
- **Surface Mount Package with RoHS Compliance**
- **MTTF > 100 years @ 85ºC ambient temperature**

Applications:

- **Telemetry**
- **Point-To-Point Radio Applications**

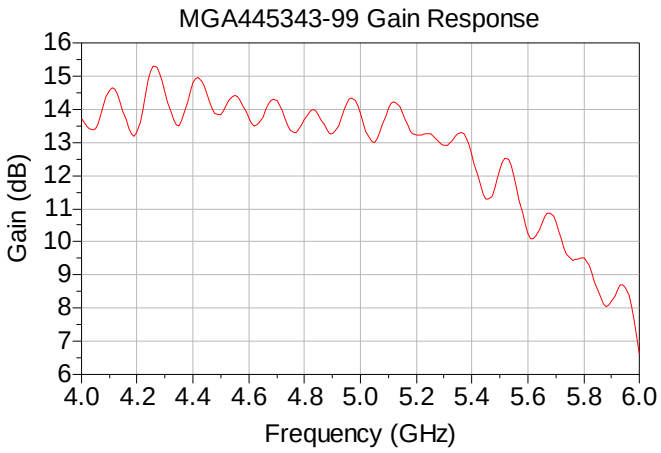
Description:

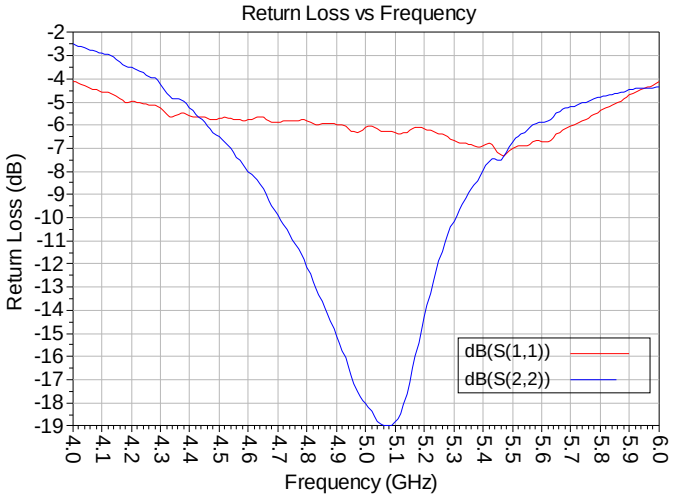
The MGA-445343-99 is a power amplifier with the State-of-the-Art linear power-added-efficiency between 4.4 GHz and 5.3 GHz frequency band. Based on advanced robust GaN device technology, the power-added-efficiency of this power amplifier is over 37% at 20 watts. At a linear burst power of 4W with 2.5% EVM and ACPR better than -38 dBc the efficiency is 20%. The modulation test pattern is 802.16x 64QAM. The high efficiency power amplifier has excellent reliability. Ideal applications include telemetry systems for driver and the output power stage, base stations back-bone, wireless infrastructures and access points. It also can be used for PTP (Point-To-Point) radio applications for this band.

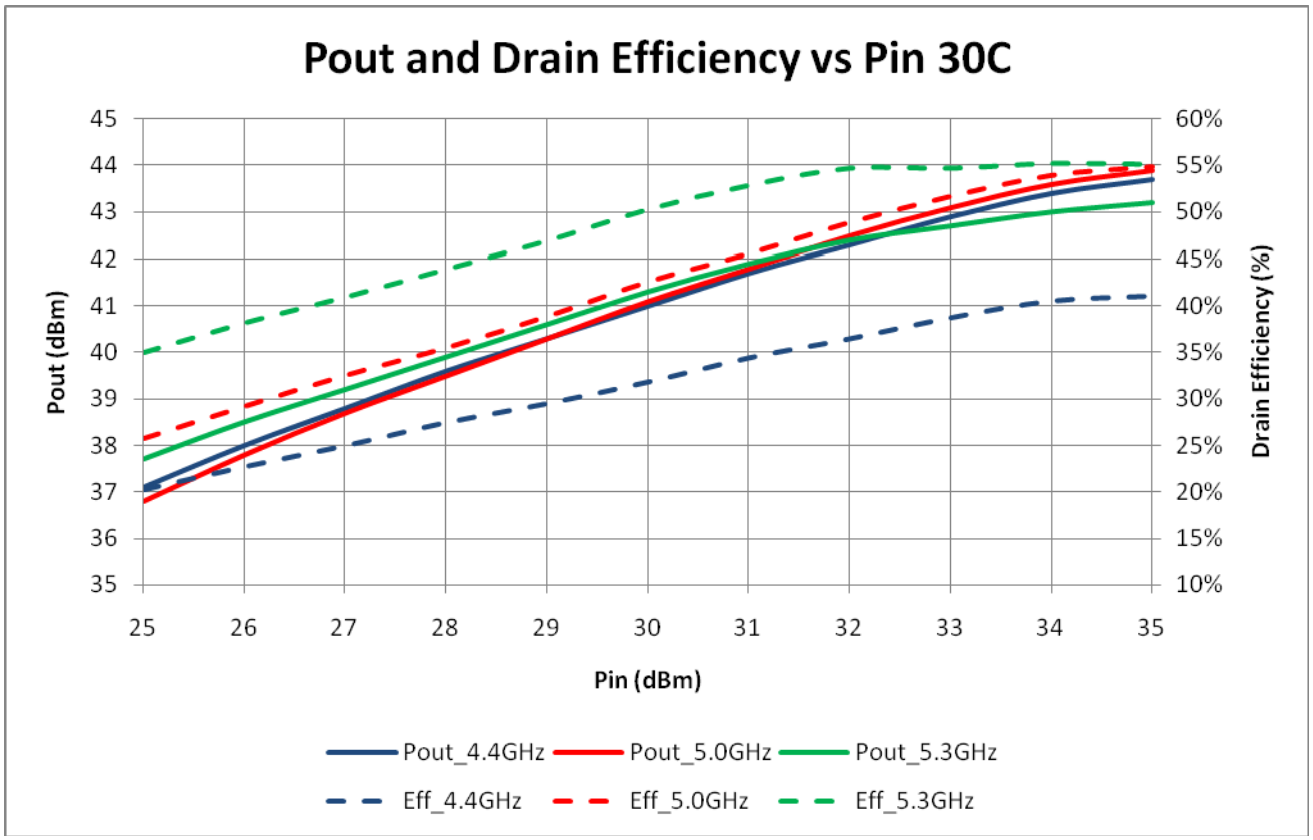
Typical RF Performance: *Vds=28V,Vgs=-2.84V, Idq=140mA, Ta=25 ºC, Z0=50 ohm*

Parameter	Units	Typical Data
Frequency Range	MHz	4400-5300
Gain (Typ / Min)	dB	14 / 12
Gain Flatness (Typ / Max)	+/-dB	1.0 / 1.5
Input Return Loss	dB	7
Output Return Loss	dB	4
Output P3dB	dBm	43
Pout @ 2.5% EVM	dBm	35
Pinch off @ Idq< 7mA	V	-4/-2.0
Operating Current Range	mA	150-300
Thermal Resistance	°C /W	4.8

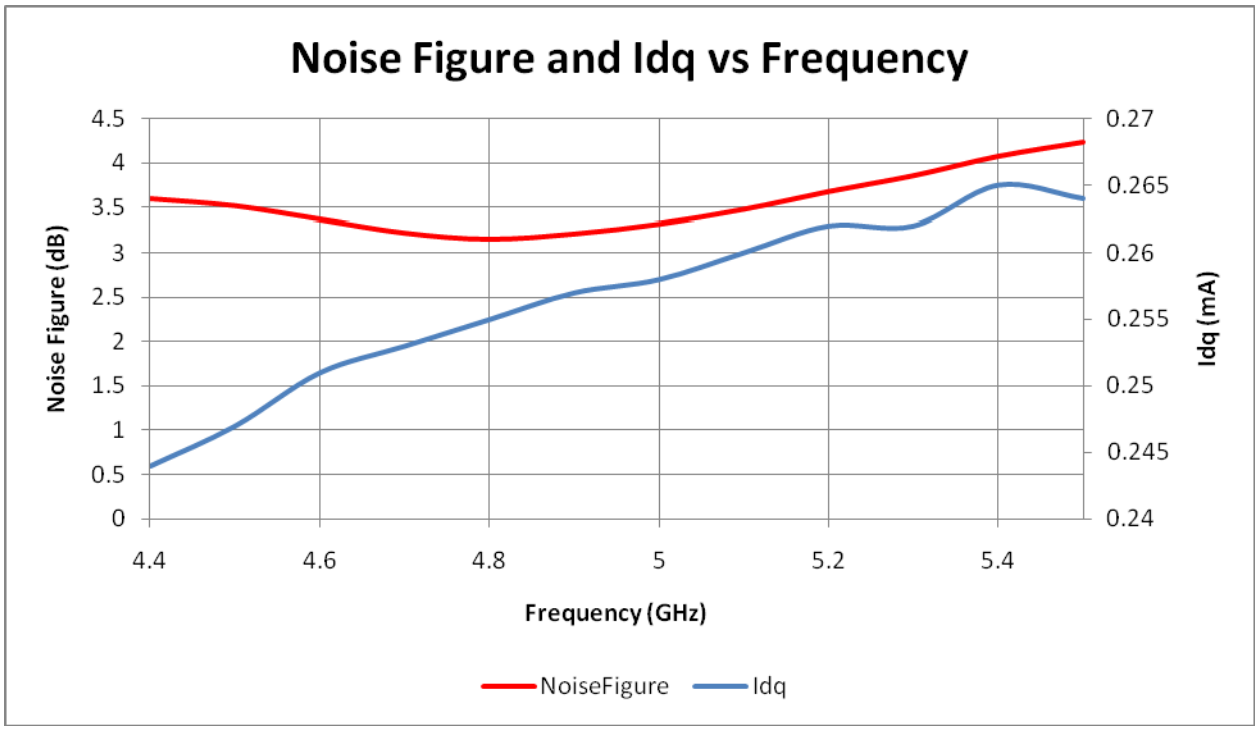
Typical RF Performance: *Vds=28.0V,Vgs=-2.84V,Idq=140mA, Z0=50 ohm, Ta=25 ºC*







Typical RF Performance(Cont'l): *Vds=28.0V,Vgs=-2.84, Idq=140mA, Z0=50 ohm, Ta=25 ºC*



Absolute Maximum Ratings: *(Ta= 25 ºC)**

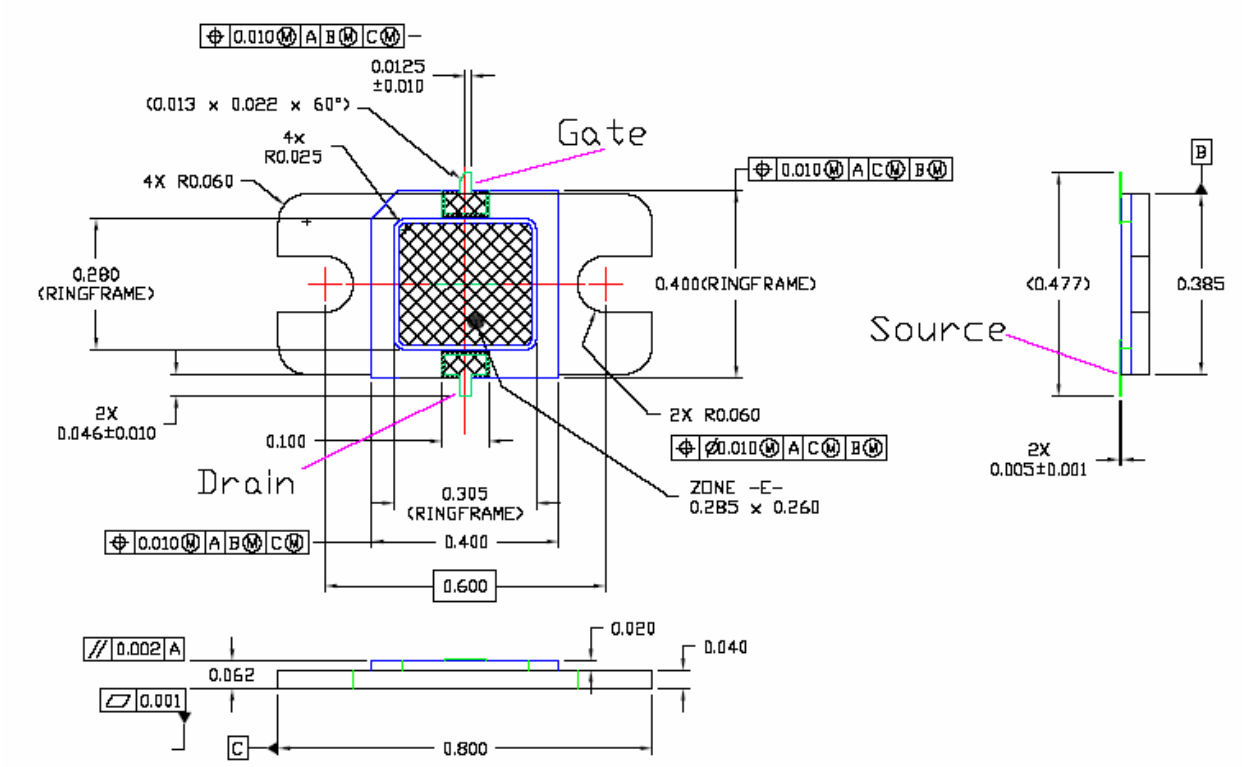
SYMBOL	PARAMETERS	UNITS	ABSOLUTE MAXIMUM
Vds	Drain-Source Voltage	V	50
Vgs	Gate-Source Voltage	V	10
Id	Drain Current	A	6
Ig	Gate Current	mA	7
Pdiss	DC Power Dissipation	W	50
Pin max	RF Input Power	dBm	+33
Tch	Channel Temperature	ºC	225
Tstg	Storage Temperature	ºC	-55 to 150

*****Operation of this device above any one of these parameters may cause permanent damage.

Typical Scattering Parameters: *Vds=28V, Vgs=-2.84V, Icq=140mA, Z0=50 ohm, Ta=25 ºC*

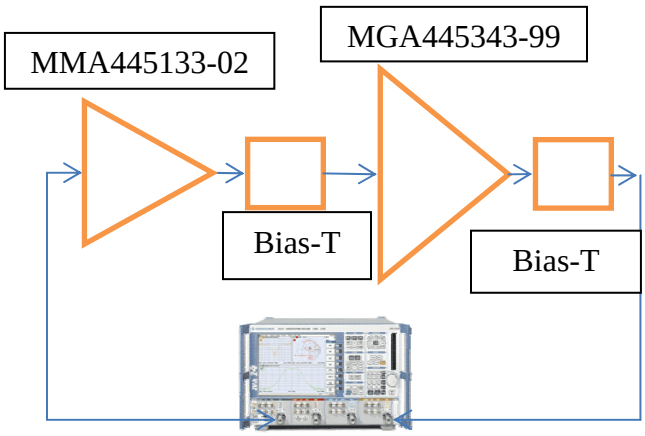
freq	magS11	AngS11	magS21	AngS21	magS12	AngS12	magS22	AngS22
4.000 GHz	0.623	4.493	4.575	-73.638	0.050	-162.788	0.750	137.023
4.100 GHz	0.592	-12.964	4.534	-80.945	0.052	-168.605	0.716	131.628
4.200 GHz	0.563	-32.025	5.426	-100.089	0.054	-167.647	0.667	125.997
4.300 GHz	0.546	-53.902	5.749	-97.794	0.055	179.268	0.615	118.265
4.400 GHz	0.526	-74.386	5.377	-119.197	0.078	168.611	0.547	112.491
4.500 GHz	0.518	-95.095	6.079	-129.533	0.080	160.456	0.472	106.621
4.600 GHz	0.514	-116.242	6.039	-138.866	0.084	142.288	0.398	98.781
4.700 GHz	0.508	-137.917	5.587	-152.705	0.076	123.381	0.320	88.533
4.800 GHz	0.511	-158.961	5.753	-166.130	0.079	111.074	0.248	76.099
4.900 GHz	0.503	-178.145	5.622	-176.210	0.072	105.375	0.175	59.361
5.000 GHz	0.494	163.573	5.164	173.287	0.061	99.134	0.125	32.823
5.100 GHz	0.483	142.191	4.945	160.794	0.071	84.512	0.114	2.424
5.200 GHz	0.493	119.648	4.941	154.875	0.079	80.784	0.193	-19.122
5.300 GHz	0.464	94.104	5.095	141.261	0.083	60.377	0.310	-48.089
5.400 GHz	0.453	70.718	4.454	132.230	0.072	46.956	0.399	-67.720
5.500 GHz	0.447	46.830	4.746	107.886	0.067	18.140	0.461	-81.275
5.600 GHz	0.461	21.473	4.300	109.609	0.064	7.679	0.509	-93.122
5.700 GHz	0.497	1.098	3.631	86.250	0.047	-3.770	0.549	-99.890
5.800 GHz	0.537	-17.746	3.434	74.906	0.040	-18.195	0.577	-105.830
5.900 GHz	0.582	-34.077	3.320	66.393	0.034	-29.089	0.597	-110.086
6.000 GHz	0.621	-48.024	2.251	56.801	0.039	-29.015	0.608	-113.576

Mechanical Information: *This Package is RoHS compliant*



All dimensions are in inches

Pin Designation (Top View)	
Pin Number	Description
Pin 1 (Chamfer)	Gate
Pin 2	Drain
Mounting Surface	GND



Application Note

The evaluation board material, not shown, is Rogers 4003 material, 20 mil thick, and 2 oz copper weight. The MGA445343-99 amplifier is bolted with #4 screws to an alumina plate with slot of 0.021 inches to recess the MGA445343-99 amplifier and keep the RF leads aligned at the same plane with the PCB interface. External bias tees from Tedica are used to provide DC to the amplifier. The driver for this amplifier is the MMA445133-02 and has small signal gain of 33 dB and P1dB of 33 dBm. The MGA445343-99 is pre-match to 50 ohms and has a peak power of 25 watts at ambient. The amplifier in the '99' package has a temperature range of approximately 85°C.

Figure 1 Test Setup

Biasing with quarter-wave stubs at the gate and drain is recommended but not shown on the evaluation unit. Via holes near the DC bias connector and amplifier will help minimizing crosstalk from neighboring circuits. A 56 ohm resistor is added in series to the gate bias. The placement of the resistor is near the 50 ohm line and the effective impedance of bias line is increased reducing RF losses on the input line and reduces the risk of video oscillations. The current from gate junction is very minimal under peak power conditions and voltage changes across the gate resistor will not cause DC instability. The MGA445343-99 has a saturated output power level of 25 Watts across the frequency range 4.4 to 5.3 GHz. The small signal gain is 13 to 14 dB with a +/- 0.75 dB ripple. The MGA445343-99 has a noise figure less than 3.0 dB. A plot of noise figure versus frequency at Idq is shown in Figure 2. At small signal levels the amplifier operates at Idq. At peak power levels 25 watts, the instantaneous voltage peaks can be 2.2 times the drain bias for drain efficiencies over 50%. Furthermore, as the output power is increased the amplifier drive current will increase. During ramp cycles, the in-rush current can be in excess of 1.5A. Careful selection of the bypass capacitors is required. A plot of Pout versus Pin over temperature is shown in Figure 4. The drain current Idd increases from 0.10 to 0.89 A and is shown in Figure 3. The RF drive level is increased incrementally and stopped when the gate leakage current of 10 mA is reached. The temperature performance for Pout vs Pin has a slope of -0.019 dB/℃. A plot of Pout vs Pin at 4.7 GHz over a temperature range from 0 to 85℃ is shown in Figure 4.

The Burst power and ACPR data are shown in Figure 5. These measurements are recorded at EVM=2.5% across the frequency range at 4.4, 4.7, 5.3 and 5.1 GHz. A WPS44492202 amplifier is used as the drive stage and has a residual EVM error of less than 0.8%. The modulation is 802.16x and each frame cycle has a 10 msec duration and runs continuously. Equalization is enabled when measuring EVM performance. The MGA amplifier bias condition is Vdd=28V and the gate voltage is adjusted for an Idq=100 mA. A diagram of test setup is shown in Figure 7 and includes the frame information about the test pattern. As the output power is backed off from the peak performance, the amplifier changes its DC/RF operation from Class 'A' to Class 'A/B'. An example of this dynamic DC/RF operation can be obverse in EVM versus Burst Power performance shown in Figure 6. The EVM is optimal at 33 dBm but not at 25 dBm in which the output power is backed off and the amplifier's operating current to reduced 150

mA. At this bias condition the amplifier is back-off near pinch off.

Applications that require gating the amplifier for TDD applications can be supported using a constant current source with a command switch to disable current loop and turnoff the amplifier as shown in Figure 9. A 1% precision resistor R8 0.2 ohm is used to convert the current to voltage. Applying KVL principal around Q2 and Q3, the current through Q2 and the load current is 30 times defined by resistor network R4 over R8. As the load current is equalized, the gate voltage to the gate of the GaN is adjusted until the voltage at Q3 base and voltage at Q2 collector is balanced. A MOSFET M2 is used to enable and disable the loop. The loop bandwidth has been intentionally truncated to minimize the loop dynamics from attacking the envelope. This allows the bias current to increase as the Pout increases; this is shown in Figure 8.

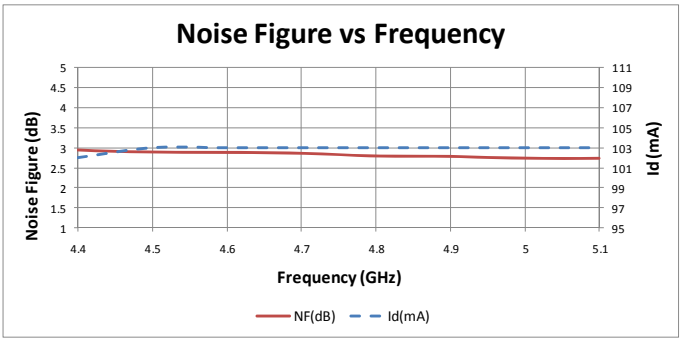


Figure 2 Noise Figure

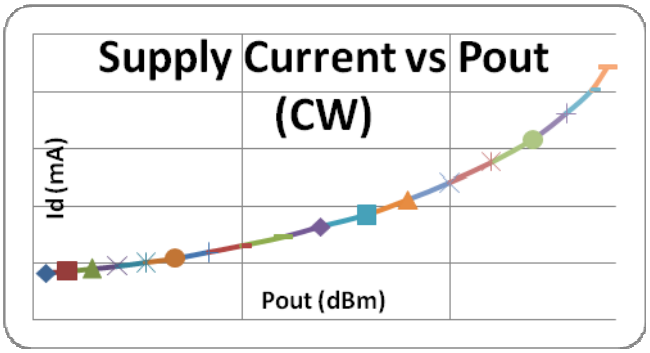


Figure 3 Supply Current

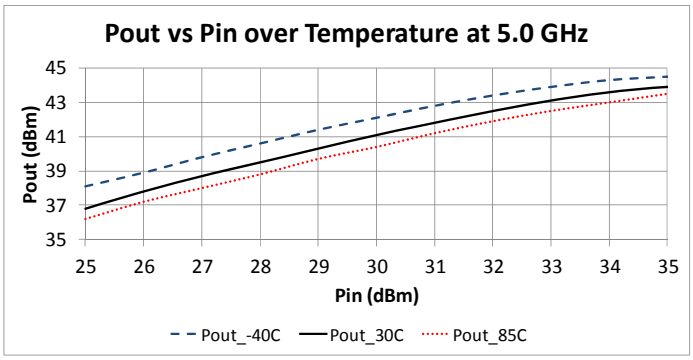
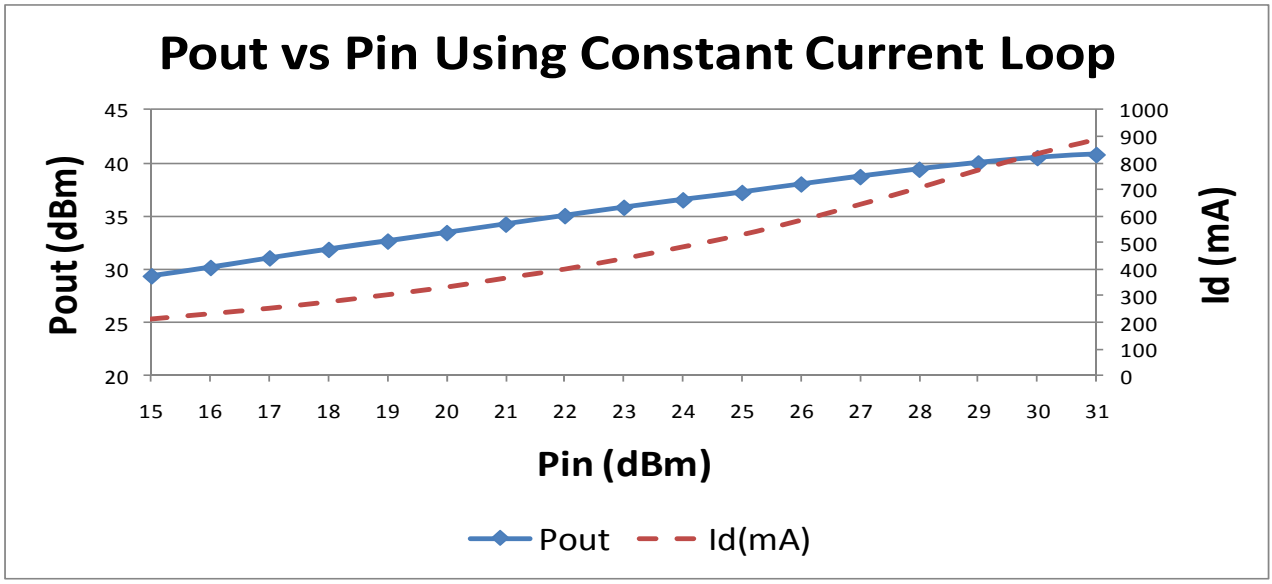


Figure 4 Pout vs Pin over Temperature

Fig 5



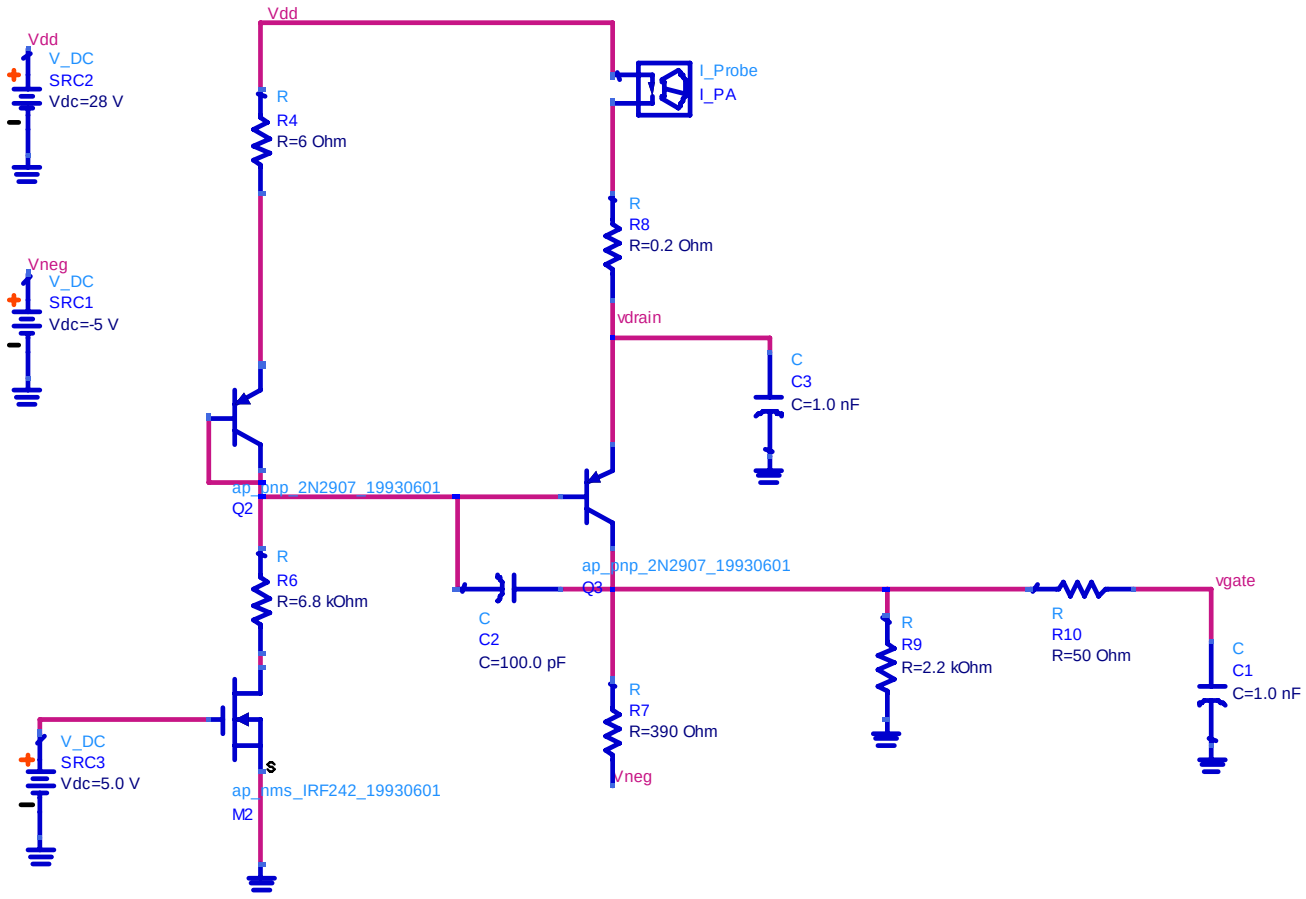


Figure 6 Schematic of Constant Current Loop